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LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for generating a current, comprising:

a first current source having a first configuration that is selectively adjusted to achieve a first current, the first current source comprising a first set of binary weighted Field Effect Transistors (FETs) coupled to provide the first current; and

a second current source having a second configuration that is selected to generate a second current that is a multiple of the first current in response to a selection of the first configuration, the second current source comprising a second set of binary weighted FETs coupled to provide the second current.

2. (Original) The system of claim 1, further comprising a precision resistor coupled between the first current source and a fixed reference voltage.

3. (Original) The system of claim 2, further comprising a current selector that determines the first current based on the voltage drop across the precision resistor and selectively adjusts ~~the~~ a first current selection signal to a desired first current.

4. (Original) The system of claim 3, the current selector provides a second current selection signal to select the second current upon achieving the desired first current.

5. (Cancelled)

6. (Currently Amended) The system of claim [[5]] 1, wherein each FET from the first set of binary weighted FETs is associated with a matching FET having a same relative binary weight from the second set of binary weighted FETs, and wherein each FET of the second set of binary

weighted FETs has a width that is K times the width of the matching FET from the first set of FETs, where K is an integer greater than one.

7. (Previously Presented) The system of claim 6, the first set of binary weighted FETs and the second set of binary weighted FETs define a current station, and further comprising a plurality of additional first set of binary weighted FETs and additional second set of binary weighted FETs defining a plurality of current stations.

8. (Original) The system of claim 7, the plurality of current stations being distributed at different locations across an integrated circuit, such that the second current is drawn more uniformly across the integrated circuit.

9. (Currently Amended) The system of claim [[5]] 1, the first set of binary weighted FETs having a common drain coupled to a first voltage and the second set of binary weighted FETs having a drain coupled to a second voltage, and further comprising a drain voltage offset compensator that compensates for the difference in drain voltage between the first and second sets of binary weighted FETs.

10. (Original) An integrated circuit comprising the system of claim 1.

11. (Original) The integrated circuit of claim 10, the first current source is associated with a reference voltage and the second current source is associated with a supply voltage of the integrated circuit.

12. (Original) The system of claim 1, further comprising a charge rationing system that employs the second current to calibrate the charge rationing system by measuring the difference with the second current source in an "OFF" state and the second current source in an "ON" state.

13. (Original) An integrated circuit comprising:

a first set of semiconductor devices configured to provide a variable current source that generates a first current based on a first binary selection signal;

a second set of semiconductor devices configured to provide a variable current source that generates a second current based on a second binary selection signal, each of the semiconductor devices of the first set of semiconductor devices having an associated matching semiconductor device from the second set of semiconductor devices that has a width that is a multiple of the width of the associated matching semiconductor device from the first set of semiconductor devices; and

a control device that determines the value of the first current and sets the second binary selection signal to provide the second current that is a multiple of the first current.

14. (Original) The integrated circuit of claim 13, the first set of semiconductor devices are coupled to a fixed reference voltage through a precision resistor and the second set of semiconductor devices are coupled to a supply voltage of the integrated circuit.

15. (Original) The integrated circuit of claim 13, the control device determines the value of the first current by measuring the voltage across the precision resistor and determines the current flowing through the precision resistor based on the measured voltage and resistance of the precision resistor.

16. (Previously Presented) The integrated circuit of claim 13, the first set of semiconductor devices comprising a first set of binary weighted Field Effect Transistors (FETs) coupled to provide the first current and the second set of semiconductor devices comprising a second set of binary weighted FETs coupled to provide the second current.

17. (Previously Presented) The integrated circuit of claim 16, further comprising a drain voltage offset compensator having at least one current correction factor to compensate for different drain

voltages associated with the first set of binary weighted FETs and the second set of binary weighted FETs, the controller employs the at least one current correction factor to determine an actual second current associated with the second variable current source.

18. (Original) The integrated circuit of claim 17, the drain voltage offset compensator comprising a drain voltage compensation table.

19. (Previously Presented) The integrated circuit of claim 18, further comprising a plurality of current stations, each of the current stations having a first set of binary weighted FETs and a second set of binary weighted FETs, the plurality of current stations being distributed at different locations across the integrated circuit.

20. (Previously Presented) A system for providing a variable current on a Very Large Scale Integrated (VLSI) circuit comprising:

means for generating a first current;

means for selectively adjusting the first current to achieve a desired first current;

means for selecting a desired second current based on the achieved desired first current;

means for generating a second current that is a multiple of the first current; and

means for compensating for differences in voltages associated with powering the means for generating a first current and the means for generating a second current.

21. (Original) The system of claim 20, the means for selectively adjusting the first current to achieve a desired first current comprising means for measuring a voltage across a precision resistor coupled to a fixed reference voltage and the means for generating a first current, and means for evaluating the first current based on the measured voltage and resistance of the precision resistor.

22. (Original) A current generation method for an integrated circuit, comprising:

generating a first current through a precision resistor;

determining the value of the first current by measuring the voltage across the precision resistor and evaluating the value of the first current based on the measured voltage and resistance of the precision resistor;

selectively adjusting the first current and determining the value of the first current until a desired first current is achieved; and

generating a second current that has a value that is a multiple of the achieved first current.

23. (Previously Presented) The method of claim 22, the generating a first current comprising selecting at least one Field Effect Transistor (FET) of a first set of binary weighted FETs, and the generating a second current comprising selecting at least one matching FET from a second set of binary weighted FETs, the at least one FET of the first set of binary weighted FETs and the at least one matching FET from the second set of binary weighted FETs having a substantially similar binary weighting.

24. (Previously Presented) The method of claim 23, further comprising determining an actual second current by compensating for a difference in drain voltage associated with the first set of binary weighted FETs and the second set of binary weighted FETs.

25. (Original) A current source comprising:

a plurality of current stations distributed over different locations on an integrated circuit, each of the plurality of current stations having a first set of semiconductor devices and a second set of semiconductor devices, each of the semiconductor devices from the first set of semiconductor devices having a matching semiconductor device from the second set of semiconductor devices that has a width that is a multiple K of the width of the corresponding matching semiconductor device of the first set of semiconductor devices;

a first select signal associated with selecting a first current to be sourced by the first set of semiconductor devices;

a second select signal associated with selecting a second current to be sourced by the second set of semiconductor devices; and

a current selector that controls the state of the first select signal and the second select signal, and selects the first current sourced by the first set of semiconductor devices and the second current source by the second set of semiconductor devices.

26. (Previously Presented) The current source of claim 25, the first set of semiconductor devices comprising a first set of binary weighted Field Effect Transistors (FETs) coupled to provide the first current and the second set of semiconductor devices comprising a second set of binary weighted FETs coupled to provide the second current.

27. (Previously Presented) The current source of claim 26, further comprising a precision resistor coupled between a fixed reference voltage and drains of the first set of binary weighted FETs of each current station, and coupling a supply voltage to drains of the second set of binary weighted FETs of each current station.

28. (Previously Presented) The system of claim 6, wherein the first set of binary weighted FETs and the associated matching FETs from the second set of binary weighted FETs are respectively activated by a first binary selection signal and a second binary selection signal, the first binary selection signal and the second binary selection signal each being a substantially similar N-bit word upon selection of the first configuration.

29. (Previously Presented) The integrated circuit of claim 13, wherein the first binary selection signal and the second binary selection signal are each binary N-bit words, and wherein the control device sets the value of each of the first binary selection signal and the second binary selection signal to be substantially similar upon determining the value of the first current.

30. (Previously Presented) The method of claim 23, wherein the generating the first current comprises activating a first N-bit binary selection signal to select the at least one FET of the first set of binary weighted FETs and the generating the second current comprises activating a second N-bit binary selection signal to select the at least one matching FET of the second set of binary weighted FETs, the first N-bit binary selection signal and the second N-bit binary selection signal being substantially similar.

31. (Previously Presented) The current source of claim 26, wherein the first select signal is a first N-bit binary signal that activates at least one FET from the first set of binary weighted FETs, and the second select signal is a second N-bit binary signal that activates at least one associated matching FET from the second set of binary weighted FETs, the first N-bit binary signal and the second N-bit binary signal having substantially similar values.